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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JOHN B. DUFFLE III, JAY S. SHAH, and BRUCE E. SINCLAIR

Appeal 2009-006308
Application 10/087,376[1]
Technology Center 2400

Before JOHN A. JEFFERY, DEBRA K. STEPHENS, and
JAMES R. HUGHES, *Administrative Patent Judges*.

HUGHES, *Administrative Patent Judge*.

DECISION ON APPEAL[2]

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[1] Application filed March 1, 2002. The real party in interest is Cisco Technology, Inc. (Br. 3.)

[2] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or for filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the "MAIL DATE" (paper delivery mode) or the "NOTIFICATION DATE" (electronic delivery mode) shown on the PTOL-90A cover letter attached to this decision.

STATEMENT OF THE CASE

Appellants appeal from the Examiner's rejection of claims 1-35 under authority of 35 U.S.C. § 134(a). The Board of Patent Appeals and Interferences (BPAI) has jurisdiction under 35 U.S.C. § 6(b).

We reverse.

Appellants' Invention

The invention at issue on appeal generally relates to a load balancing method for parallel coprocessors by determining an anticipated load on the coprocessors. (Spec. 1:3-4; 4:10-16.)[3]

Representative Claim

Independent claim 1 further illustrates the invention, and is reproduced below with the key disputed limitations emphasized:

> 1. A method for selecting a coprocessor from a plurality of coprocessors to process a packet, the method comprising steps of:
>
> determining a size of the packet;
>
> *determining a cost associated with the packet* in response to the size of the packet, *the cost representing a load associated with processing the packet*;
>
> *determining an anticipated load for each coprocessor in the plurality of coprocessors using the cost*; and
>
> *selecting the coprocessor from the plurality of coprocessors based on the anticipated load.*

[3] We refer to Appellants' Specification ("Spec.") and Appeal Brief ("Br.") filed February 5, 2008. We also refer to the Examiner's Answer ("Ans.") mailed March 26, 2008.

References

The Examiner relies on the following references as evidence of unpatentability:

Feinberg	US 6,065,046	May 16, 2000
Robertazzi	US 6,370,560 B1	Apr. 9, 2002 (filed Mar. 13, 1998)
Modi	US 6,587,866 B1	Jul. 1, 2003 (filed Jan 10, 2000)

Rejections on Appeal

The Examiner rejects claims 1-9, 13, 14, 17, 21-27, 31, and 32 under 35 U.S.C. § 102(e) as being anticipated by Robertazzi.

The Examiner rejects claims 10-12, 15, 16, 18-20, 28, 29, 33, and 34 under 35 U.S.C. § 103(a) as being unpatentable over the combination of Robertazzi and Modi.[4]

The Examiner rejects claims 30 and 35 under 35 U.S.C. § 103(a) as being unpatentable over the combination of Robertazzi, Modi, and Feinberg.

ISSUE

Based on our review of the administrative record, Appellants' contentions, and the Examiner's findings and conclusions, the pivotal issue before us is as follows:

Does the Examiner err in finding Robertazzi discloses: (1) determining a cost associated with the packet in response to the size of the

[4] The Examiner includes claims 30 and 35 in the statement of rejection. We revise the statement of the Examiner's rejection to eliminate this harmless typographical error.

packet, the cost representing a load associated with processing the packet; (2) determining an anticipated load for each coprocessor in the plurality of coprocessors using the cost; and (3) selecting the coprocessor from the plurality of coprocessors based on the anticipated load?

FINDINGS OF FACT (FF)

Robertazzi Reference

1. Robertazzi generally describes load sharing a divisible task among multiple processors to optimize computation time, and a controller for performing load sharing. (Col. 1, l. 16 to col. 2, l. 19.)

2. Robertazzi also describes simultaneously (parallel) processing a divisible task or load among multiple processors to optimize the monetary cost of processing the task within a defined processing time. (Col. 3, ll. 9-14; col. 4, ll. 7-63; col. 4, l. 66 to col. 5, l. 7; col. 5, ll. 18-61; col. 8, ll. 5-50; col. 11, l. 6 to col. 12, l. 39.)

3. In particular, Robertazzi describes determining the size of a task (load) and dividing the task into segments for processing by different processors. (Col. 8, ll. 5-50; col. 11, ll. 21-27, 46-64.) Robertazzi describes determining the speed of various processors (col. 2, ll. 9-19; col. 4, ll. 18-30; col. 8, ll. 5-50; col. 11, ll. 52-64), and determining the size of a segment of the task based on the available time in which a processor can process the segment (col. 8, ll. 5-50; col. 11, ll. 21-27, 46-64) – "[t]he load or task will be divided so that the segment will fully utilize the cheapest processor for the entire selected finish time constraint" (col. 8, ll. 38-41) – i.e., determining the utilization time (cost) for a particular task segment on a particular processor. Robertazzi also describes determining the monetary

cost associated with the processing of a load and optimizing (minimizing) the cost by determining the unit cost associated with each processor (col. 4, ll. 14-59), and dividing a task so as to process the task segments on the least expensive available processor (col. 8, ll. 5-50; col. 11, ll. 21-27, 46-64), i.e., Robertazzi selects the processor for processing a segment based on the utilization cost and monetary cost.

ANALYSIS

Appellants have the opportunity on appeal to the Board of Patent Appeals and Interferences (BPAI) to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) (citing *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)). The Examiner sets forth a detailed explanation of a reasoned conclusion of anticipation in the Examiner's Answer with respect to Appellants' claims 1-9, 13, 14, 17, 21-27, 31, and 32 (Ans. 3-8, 13-18), and in particular independent claim 1 (Ans. 3, 13-18). The Examiner also sets forth a detailed explanation of a reasoned conclusion of obviousness in the Examiner's Answer with respect to Appellants' claims 10-12, 15, 16, 18-20, 28-30, and 33-35. (Ans. 8-13, 18-26.) Therefore, we look to the Appellants' Brief to show error in the proffered reasoned conclusions. *See Kahn*, 441 F.3d at 985-86.

Arguments Concerning the Examiner's Rejection of Representative Claim 1

The Examiner rejects Appellants' independent claim 1 as being anticipated by Robertazzi. (Ans. 3.) Appellants' representative claim 1 calls for, in pertinent part: (1) determining a cost associated with the packet in response to the size of the packet, the cost representing a load associated

with processing the packet; (2) determining an anticipated load for each coprocessor in the plurality of coprocessors using the cost; and (3) selecting the coprocessor from the plurality of coprocessors based on the anticipated load. (Br. 21, Claim App'x., Claim 1.) Based on the record before us, we find error in the Examiner's anticipation rejection of Appellants' claim 1. We agree with Appellants that Robertazzi does not disclose the disputed features of at least "determining an anticipated load for each coprocessor in the plurality of coprocessors using the cost," and "selecting the coprocessor from the plurality of coprocessors based on the anticipated load" (Br. 21) for essentially the reasons espoused by Appellants (Br. 12-14).

The Examiner finds that Robertazzi discloses each feature of Appellants' claim 1, including: "determining the size of the packet" (citing col. 4, ll. 7-59); "a cost associated with the packet, the cost representing a load associated with processing the packet" (citing col. 4, ll. 7-59; col. 11, ll. 5-28); "determining an anticipated load for each coprocessor in the plurality of coprocessors using the cost" (citing col. 4, ll. 7-59; col. 11, l. 5 to col. 12, l. 39); and "selecting the coprocessor [selected processors] from the plurality of coprocessors based on the anticipated load" (citing col. 4, ll. 7-59; col. 11, l. 5 to col. 12, l. 39). (Ans. 3.) Additionally, the Examiner responds that "Robertazzi discloses 'a load sharing system which minimizes overall costs by assigning segments of a divisible load to distributed processor platforms based on the resource utilization cost of each processor platform.'" (Ans. 13-14 (quoting Abstract).)

The Examiner also responds that:

> Each different type of processor platform has an associated resource utilization cost when used to process a portion of a load [Each processor has a different utilization

> cost, please note, utilization cost, not monetary cost]. . . . The resource utilization cost of a processor includes factors such as the monetary computing cost whose unit is "cost per second" and the computing speed whose unit is "loads/tasks per second".

(Ans. 15-16.) The Examiner further responds that:

> Robertazzi clearly discloses selecting a coprocessor based on anticipated load. In column 11, line 5 - column 12, line 39, Robertazzi discloses Figure 4 of the invention where Robertazzi discloses "calculating overall cost of the divisible job to be distributed among the available processor platform in the network." Robertazzi also discloses that "Task size can be computed based on such factors as the complexity of the task and the necessary data inputs. The cost is minimized by placing as much of the load or task on the processor platforms with associated data links having a relatively low resource utilization cost while still completing the processing within an acceptable finish time" and compares "the calculated overall cost is greater than the selected cost constraint" to make determination to "reallocates an incremental portion of the load from the most expensive processor platform to the cheaper processor platforms (which reduces cost but most likely decreases speed) and also "distributes the load to the selected processor platforms using the determined allocation in the previous steps."

(Ans. 17.)

Appellants contend, *inter alia*, that:

> Robertazzi does not teach the Applicant's claimed "*determining an anticipated load for each coprocessor*" and "*selecting the coprocessor from the plurality of coprocessors based on the anticipated load*."
>
> . . . The Applicant defines *anticipated load* at page 9, lines 5-6 of the specification stating "anticipated load is the load a coprocessor would incur if it were to process the packet given its current load." The Applicant then selects a coprocessor "*based on the anticipated load*."

> Robertazzi lacks any metric akin to the claimed anticipated load, and thus does not select processing platforms based on it. Instead, Robertazzi looks to monetary costs, assigning tasks to processing platforms trying to achieve the cheapest price. Each processing platform in Robertazzi is simply characterized as "available" or "busy." See Robertazzi Fig. 1C, 183. Robertazzi fails to determine how much more busy a processing platform would be if it were to process a task given its current load, nor does Robertazzi base any selection upon this.

(Br. 13-14.)

As explained by Appellants, claim 1 includes a limitation requiring determining an anticipated load for each coprocessor and then selecting one of the coprocessors based on the anticipated load (in order to balance the loads placed on the coprocessors – *see* Spec. 4:10-16). The Examiner finds that Robertazzi discloses these features citing column 4, lines 7-59 and column 11, line 5 to column 12, line 39 as describing this feature. (Ans. 3, 17.)

As detailed in the Findings of Fact section *supra*, we agree with the Examiner that Robertazzi discloses load sharing and parallel processing a divisible load among multiple processors to optimize the monetary cost of processing the task within a defined processing time, by determining: the size of the load and dividing the task into segments for processing by different processors, the speed of various processors, the size of a segment of the load, the utilization time (cost) for a particular load segment on a particular processor, the monetary cost associated with the processing of a load, and optimizing the cost. (FF 1-3.) In summary, Robertazzi selects a

processor for processing a load segment based on the utilization cost and monetary cost.

In selecting the processor, we find that Robertazzi discloses determining the size of a portion of the load (load segment) to fully utilize the processor for a constrained period of time (FF 3) – which we find discloses determining an anticipated load for a particular selected processor. However, Robertazzi makes the determination of which processor to select based on the "resource utilization cost" (monetary cost (cost/sec) and computing speed (load/sec)), and then determines the anticipated load on the processor. (*See* FF 3.) Only if the load can not be processed within a constrained time period does the controller share the load to other more expensive processors. (*Id.*) Therefore, we disagree with the Examiner that Robertazzi describes determining an anticipated load for each coprocessor. Robertazzi describes sharing a load across multiple computing platforms and processors, and certainly does not disclose determining the anticipated load for each such processor. (*See* FF 1-3.) Robertazzi, at most, describes selecting a processor out of all accessible processors based in part on the cost associated with processing the load on the processor, determining the anticipated load on the processor, and then, in order to meet a time constraint, sharing the load with additional processors selected in the same way. (*See* FF 3.)

Thus, we are constrained by the record before us to agree with Appellants that Robertazzi does not disclose at least the disputed features of "determining an anticipated load for each coprocessor" and "selecting the coprocessor from the plurality of coprocessors based on the anticipated

load." It follows that Appellants have persuaded us to find error in the Examiner's anticipation rejection of Appellants' independent claim 1.

Appellants' independent claims 17, 21, 22, 23, 26, and 31 include the limitations of similar scope. Thus, based on the record before us, we find that the Examiner erred in finding Robertazzi discloses each limitation recited in Appellants' claims 1-9, 13, 14, 17, 21-27, 31, and 32. Accordingly, we reverse the Examiner's anticipation rejection of these claims.

The Examiner's Rejection of Claims 10-12, 15, 16, 18-20, 28-30, and 33-35 Under 35 U.S.C. § 103(a)

The Examiner rejects Appellants' dependent claims 10-12, 15, 16, 18-20, 28, 29, 33, and 34 as being unpatentable over the combination of Robertazzi and Modi. (Ans. 8-11; *see* note 4 (*supra*).) Claims 10-12, 15, and 16 depend on claim 1. Claims 18 and 20 depend on claim 17. Claims 28 and 29 depend on claim 26. Claims 33 and 34 depend on claim 31. The Examiner also rejects Appellants' dependent claims 30 and 35 as being unpatentable over the combination of Robertazzi, Modi, and Feinberg. (Ans. 12-13; *see* note 4 (*supra*).) Claim 30 depends on claim 26. Claim 35 depends on claim 31. For the reasons explained with respect to claim 1 (*supra*), we find Robertazzi does not disclose, teach, or suggest each feature of these claims. Modi and Feinberg do not cure the deficiencies of Robertazzi. Therefore, based on the record before us, we find that the Examiner erred in finding Robertazzi and Modi would have collectively taught or suggested each limitation recited in Appellants' claims 10-12, 15, 16, 18-20, 28, 29, 33, and 34. Similarly, we find that the Examiner erred in finding Robertazzi, Modi, and Feinberg would have collectively taught or

suggested each limitation recited in Appellants' claims 30 and 35. Accordingly, we reverse the Examiner's obviousness rejection of claims 10-12, 15, 16, 18-20, 28-30, and 33-35.

CONCLUSIONS OF LAW

Appellants have shown that the Examiner erred in rejecting claims 1-9, 13, 14, 17, 21-27, 31, and 32 under 35 U.S.C. § 102(e).

Appellants have shown that the Examiner erred in rejecting claims 10-12, 15, 16, 18-20, 28-30, and 33-35 under 35 U.S.C. § 103(a).

DECISION

We reverse the Examiner's rejection of claims 1-9, 13, 14, 17, 21-27, 31, and 32 under 35 U.S.C. § 102(e).

We reverse the Examiner's rejection of claims 10-12, 15, 16, 18-20, 28-30, and 33-35 under 35 U.S.C. § 103(a).

REVERSED

msc

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